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Wireless LAN – A Unified Physical Layer Design and Measurement Environment

March 6, 2002

presented by:

Speaker #1 Joe Troychak

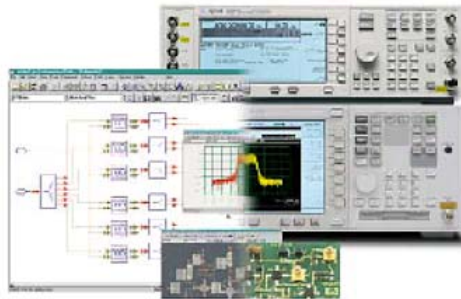
Speaker #2 Afshin Amini

Introduction

- **Growing demand for Wireless Networking signals**
 - IEEE 802.11a/b WLAN and Bluetooth standards
- **Design & Verification requirements**
 - Ideal and impaired signals (for design and emulation)
 - Leverage signals across simulation and test domains
- **Agilent Connected Solutions**
 - Advanced Design System (ADS)
 - Vector Signal Analyzer (VSA) - recordings and analysis
 - Electronic Signal Generator (ESG) – signal source

Agilent Portfolio - EDA and Instrument

• Connected Solutions



Simulation Models



Connected Solutions

Unique Features and Benefits

- One environment, one design database, one user interface for Mixed Signal System Design and simulation
- Generate complex signals, apply to hardware to measure prototype data, send results to ADS for comparison
- Gain insight into design behavior by comparing simulations to measured prototypes for troubleshooting
- Integrate measured data and instrument algorithms into ADS, and use simulation models and signals for verification tests

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Simulating and testing modern wireless radio systems requires accurate generation of complex modulated RF signals. Examples include third-generation (3G) cellular and wireless networking applications such as Bluetooth and wireless local area networking (WLAN). Simulation can help validate prototype IC designs early, resulting in shorter design cycles and faster production times. Obtaining good correlation between simulated and measured data provides for a closed loop design cycle. Moving complex signals, data, and test vectors between simulation and measurement domains further shortens the design cycle.

Simulating and testing a WLAN 802.11a receiver requires transmit packet bit-level accuracy of short and long preambles, signaling, and data contents. This transmit packet information is used for receiver phase, frequency, and timing adjustments. It is necessary for the receiver to operate in severe multi-path environments, and advantageous to perform simulations and measurements including multi-path distortion. Power amplifiers for 802.11a must meet linearity requirements for signals with peak-to-averages in excess of 10 dB. Simulating and testing with exactly the same complex modulated signals helps ensure that amplifier results correlate.

This paper will highlight virtual measurements within ADS simulations, and demonstrate hardware emulation using GPIB hardware links to an Agilent ESG IQ arbitrary waveform generator. Arbitrary IQ signals can originate in either the simulation or measurement domains, and captured for reuse within system level design, integration, and test. Results are recorded with an Agilent Vector Signal Analyzer (VSA) for reuse in simulations for evaluating hardware prototype designs and post-processing measured data.

Design Challenges of OFDM Modulation

- Frequency offset - receiver corrections
- Oscillator phase noise - clean and stable
- IFFT/FFT - fixed point implementation
- Inter-symbol Interference (ISI) - multi-path and guard interval requirements
- OFDM peak to average ratio – power amplifier drive level, power efficiency.



1,2)Effect:

Frequency offset and phase noise both produce Inter-Carrier Interference (ICI). This ICI degrades the ability of the receiver (FFT) to distinguish between sub-carriers, i.e. Orthogonality is destroyed.

Likely Cause: oscillator

SO Designer need to be able to simulate and analyze the impact of oscillator and circuit designer need to know the boundary of design parameters. The engineer working on the Receiver needs to be fully aware of frequency synchronization and phase tracking algorithms and impact of RF front end and how to work them together

3)Effect:

Fixed point processing produces uncertainty due to the quantization effects imposed on the modulated symbols as signal get processed through the IFFT and FFT.

Likely Cause: poor choice of digital HW

SO Designer need to be able to choose the HW that gives him best tradeoff between power/size visavis signal fidelity.

4) Effect:

Multipath causes ISI- it is mitigated with extending each subcarrier beyond the symbol time called Guard Interval: IEEE802.11a has a 800 nsec GI

Likely cause: outdoor channel-mobility

SO designer Beyond 800 nsec need to have an environment to quickly analyze the signal degradation caused by multipath

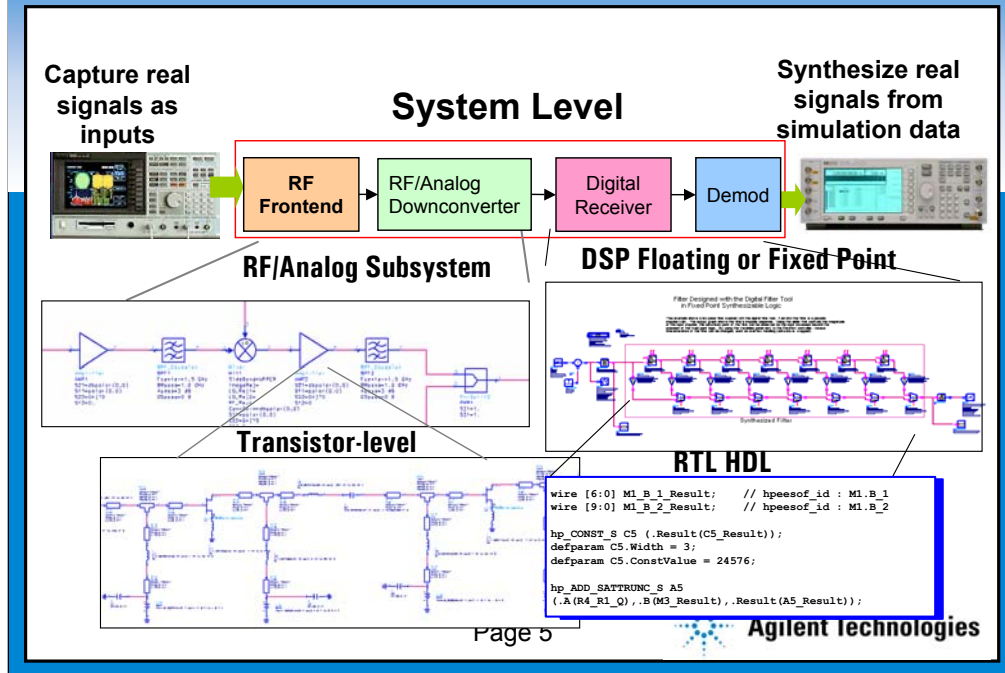
5) Effect

PA Operating in the non-linear region causes signal degradation- back off causes inefficiency in power

Likely cause: no cause- NEED a great PA design! That works in your system

SO PA and system designer designers need an integrated environment to be able to design and simulate and verify their circuit and test the HW in a consistent way

ADS Top-Down Design Methodology



NEED:

INTEGRATED DESIGN ENVIRONMENT

Once design requirements flow down from **SYSTEM** to RF and DSP designers, they can begin working on detailed circuit and DSP designs. The top level system design can then be used as a template for evaluating the effects of a circuit or DSP design on the overall system performance for bottoms-up verification.

For example, let's say that you are designing a 5 GHz PA to be used in a 802.11a transmitter which has a certain modulation accuracy specification. This is not an intuitive specification for the PA designer... However, the detailed PA circuit design, could be inserted back into the top level design to evaluate how the PA performance impacts the overall modulation accuracy performance.

This ability to mix levels of abstraction, using detailed RF circuit and DSP designs, when available, and functional elements when detailed designs aren't available, allows the overall system performance to be evaluated at every stage in the design process to reduce risk.

ADS's link to test instrumentation provides a final level of abstraction, where the measured performance of a hardware prototype can be inserted back into the top level system to evaluate it's effect on the overall system performance.


IEEE802.11 PHY Layer

SYSTEM	FREQUENCY BAND	MAX DATA RATES (MBPS)	TRANSMIT SCHEME			MODULATION			
			CCK	PBCC	OFDM	BPSK	QPSK	16QAM	64QAM
802.11b	2.4GHz	11		Option		Diff.	Diff.		
802.11g	2.4GHz	54		Option		Diff.	Diff.		
802.11a,h	5GHz	36, option to 54							
HiperLAN/2	5GHz	54							
HiSWAN	5GHz	54							



5 GHz WLAN Design Library & DesignGuide

IEEE <u>Library</u>	IEEE <u>DesignGuide</u>
<ul style="list-style-type: none">• IEEE 802.11a<ul style="list-style-type: none">• Complete TX and RX models• PA Test & Verification project• TX and RX Test and verification projects include receiver sensitivity, adjacent Channel rejection, phase noise degradation, fading and other distortions• Measurements include:<ul style="list-style-type: none">• EVM, Output RF spectrum, CCDF, BER/PER• Hiperlan/2<ul style="list-style-type: none">• PA Test & Verification• Complete TX models	<ul style="list-style-type: none">• IEEE 802.11a<ul style="list-style-type: none">• Link impairment tests include Frequency offset between TX and RX, Oscillator phase noise, fixed point effect in FFT/IFFT• Zero-IF receiver tests include LO leakage/DC offset compensation, AGC, Receiver adjacent/alternate channel

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Emerging markets- low mobility wireless

Agilent E8874A 5 GHz WLAN Design Library

The 5 GHz WLAN Design Library from Agilent EEs of EDA lets designers successfully develop high data rate Wireless LAN communications products based on the IEEE802.11a and Hiperlan2 standards. With this library, designers develop and refine specification-compliant algorithms at the system level, where design choices have the greatest impact, and quickly move designs to implementation.

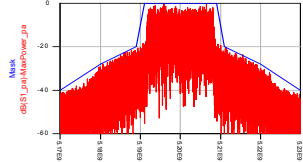
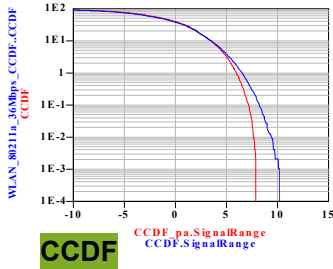
The 5 GHz WLAN Design Library is designed for use with Agilent's Advanced Design System 2001(ADS 2001), the powerful EDA design and simulation software package for communication system, RF and microwave designers of all types. The library includes pre-configured test and verification setups for evaluating designs and testing performance parameters such as Output RF Spectrum, Error Vector Magnitude (EVM), Power Statistics using Complementary Cumulative Distribution Function (CCDF), and Bit Error Rate/ Packet Error Rate (BER/PER) for the IEEE802.11a standard. Hiperlan2 transmitter models and test and verification setups help designers evaluate Output RF Spectrum, ACPR, and Power Statistics using the Complementary Cumulative Distribution Function (CCDF).

For more information about the 5 GHz WLAN Design Library or ADS 2001, visit www.agilent.com/eesof-eda.

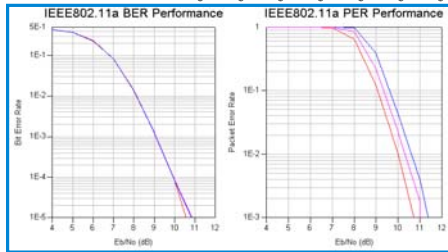
Measurements

D: Ch1 OFDM Syms/Errs		RMS:7	Range: 12 dBm
EVM	= -27.798 dB	EVM	= 4.0747 %rms
PilotEVM	= -29.067 dB	CPE	= 1.0094 %rms

EVM



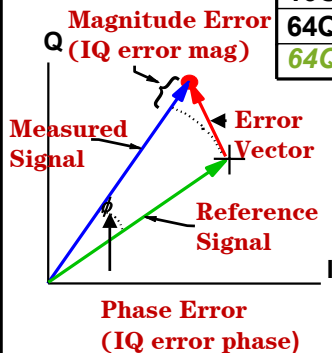
ORFS



BER/PER

EVM- IEEE802.11a spec

Mod	**Rate	EVM, dB	*EVM, %
BPSK	6	-5	56.2
BPSK	9	-8	39.8
QPSK	12	-10	31.6
QPSK	18	-13	22.3
16QAM	24	-16	15.8
16QAM	36	-19	11.2
64QAM	48	-22	7.9
64QAM	54	-25	5.6



$$*EVM \% = 100 * 10^{(EVM_{dB}/20)}$$

** Mb/s

“Error Vector Magnitude” (EVM) as a measure of modulation quality. This metric has become an industry standard for a wide variety of applications from cellular to cable television. The basic idea behind EVM is that any impaired signal (usually complex signals) can be represented as the sum of an ideal signal and an error signal. Since the error signal can’t be measured directly, the test instrumentation determines the error signal by reconstructing the ideal signal based on the detected data and subtracting it from the actual signal.

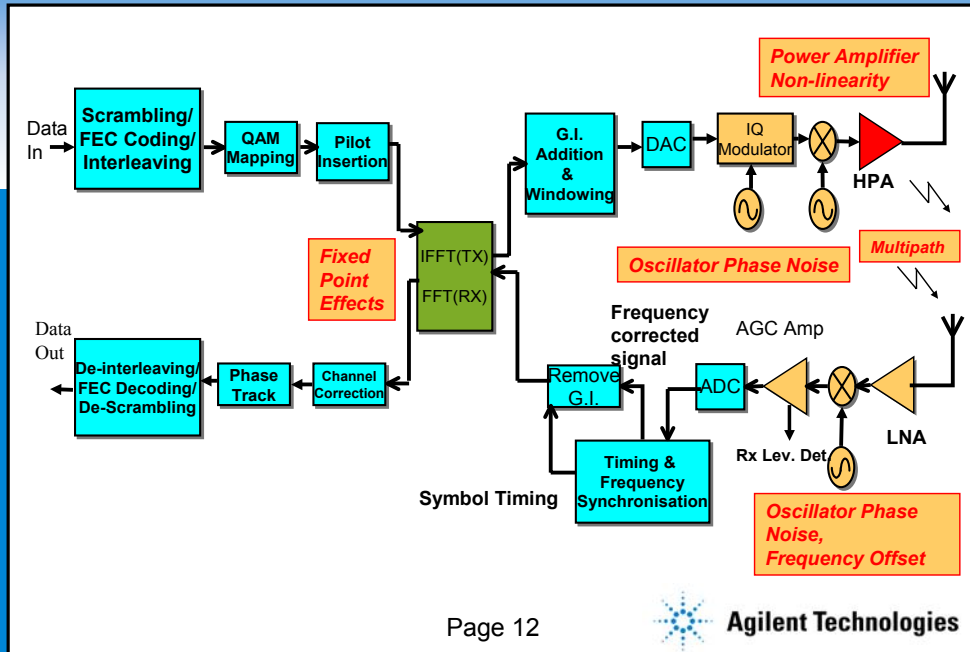
The error signal includes all sources of error including:

- Additive Noise
- Nonlinear distortion
- Linear Distortion (equalized in 802.11A)
- Phase Noise
- Spurious
- Other Modulation errors

Table shows the IEEE802.11a standard modulation quality in terms of EVM

In the table we have highlighted the percentage EVM at rates of 24Mb/s which uses 16QAM for sub-carrier modulations and 54 Mb/s that uses 64QAM- it can be seen from table at higher data rates the EVM becomes smaller as a result of tighter constellation points.

OFDM Transceiver-- Impairments



We saw the EVM numbers in the previous slides-

Now let's take a look at a transceiver path and correlate the impairment with the the likely cause.

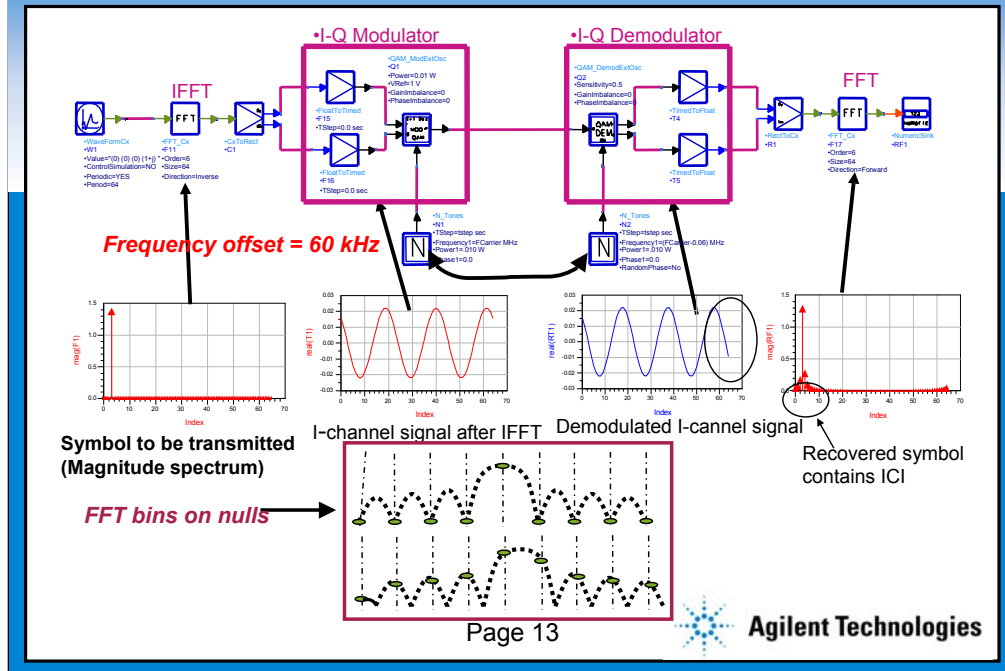
NEED MODELS THAT SATISFY EVOLVING SPECS

We talked about the 5 main design challenges of OFDM.

We need set of models that we could easily use to create coded signals at various data rates of IEEE802.11a, namely: 6-54 Mb/s and beyond

We also need set of models to detect and demodulate each of these signals and finally gives BER and PER(Packet Error rate)

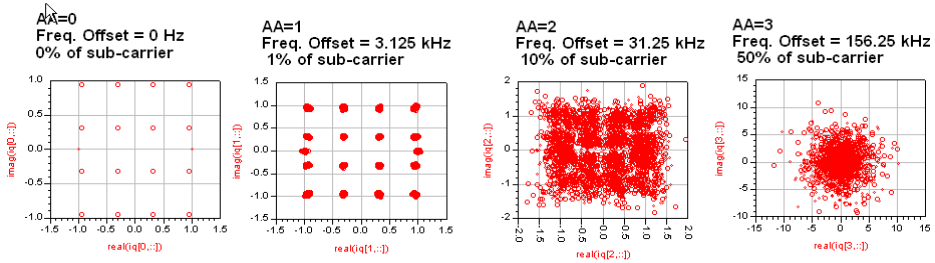
OFDM Operation (ICI problem)



Frequency offset skews the sub-carrier in frequency which causes spectral leakage in the receiver's FFT. This leakage forces energy from one sub-carrier to fall inside the FFT bin of adjacent sub-carrier bins. This is what produces ICI.

This diagram shows how critical receiver frequency tracking is. If the receiver is off frequency, then the nulls in each carrier won't land on an FFT bin. In FFT terminology this is called leakage. For OFDM, the result is inter-carrier interference.

Frequency Offset-No Synchronization

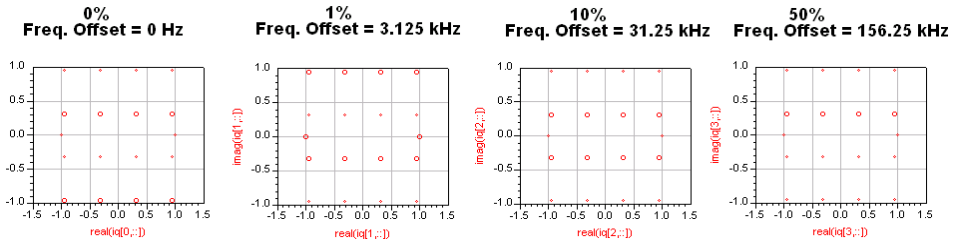


Index	ReceiverEVM
AA=0.000	1.198E-5
AA=1.000	0.025
AA=2.000	0.268
AA=3.000	2.840

Freq. Offset / Freq. Spacing

- 0% **Why you need frequency offset correction:**
- 1% **assume freq. offset=3kHz (1%),**
- 10% **requires:**
- 50% **oscillator stability 3k/5.8G=0.5ppm!**

Frequency Offset-Synchronization

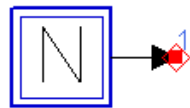


Index	ReceiverEVM	Freq. Offset / Freq. Spacing	
AA=0.000	40	1.199E-5	0%
AA=1.000	40	1.214E-5	1%
AA=2.000	40	1.211E-5	10%
AA=3.000	40	1.210E-5	50%

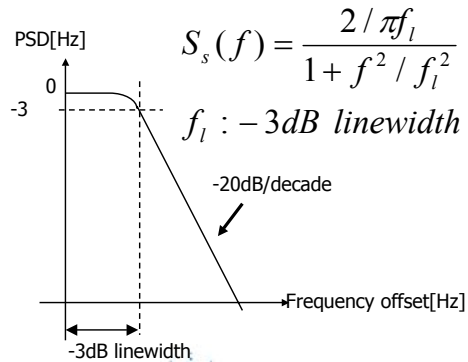
Oscillator Phase Noise

- **N_Tones** model is used to model the phase noise
- **Based on Lorentzian spectrum**
- **Characterized by -3dB-linewidth, -20dB per decade slope**

Phase noise profile based on Lorentzian spectrum



N_Tones
N2
Frequency1=FCarrier MHz
PhaseNoiseData=PN



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The power spectrum density of an oscillator signal with phase noise is modeled by a Lorentzian spectrum- it shows a squared magnitude of a first order LPF function.

Reference: R. van Nee et al. OFDM For Wireless Multimedia Communications Artech House 2000

Random phase variation:

Phase tracking in the receiver can remove phase noise at very low frequencies that basically looks like a uniform shift in phase across all sub-carriers. This is accomplished during every OFDM symbol by monitoring the pilot signals.

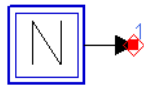
In any ideal receiver phase tracking will track this out-i.e.. VSA software Phase Tracking option

The more disturbing problem is ICI- studies show that with a phase noise profile as shown the 3 dB phase noise BW should be at the order of 0.01% of the sub-carrier spacing i.e.. 30 Hz for 312 KHz

Phase lock effects are not presented but can be simulated using the circuit representation and co-simulation power of ADS

Phase Noise model

- 3 profiles of phase noise were simulated:



N_Tones
N2
Frequency1=FCarrier MHz
PhaseNoiseData=PN

VAR

VAR4

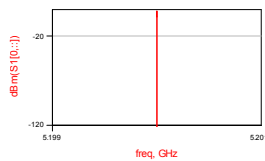
AA=1

PN0=""

PN1="" 120 -15 300 -23 3000 -43 30000 -63 300000 -83 1200000 -95"

PN2="" 120 -35 300 -43 3000 -63 30000 -83 300000 -103 1200000 -115"

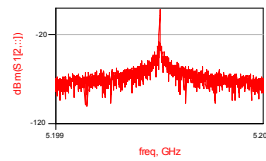
PN=f (AA=0) then PN0 elseif (AA=1) then PN1 else PN2 endif



Ideal



-3dB linewidth=30Hz
0.01% of sub-carrier spacing



-3dB linewidth=3Hz
0.001% of sub-carrier spacing

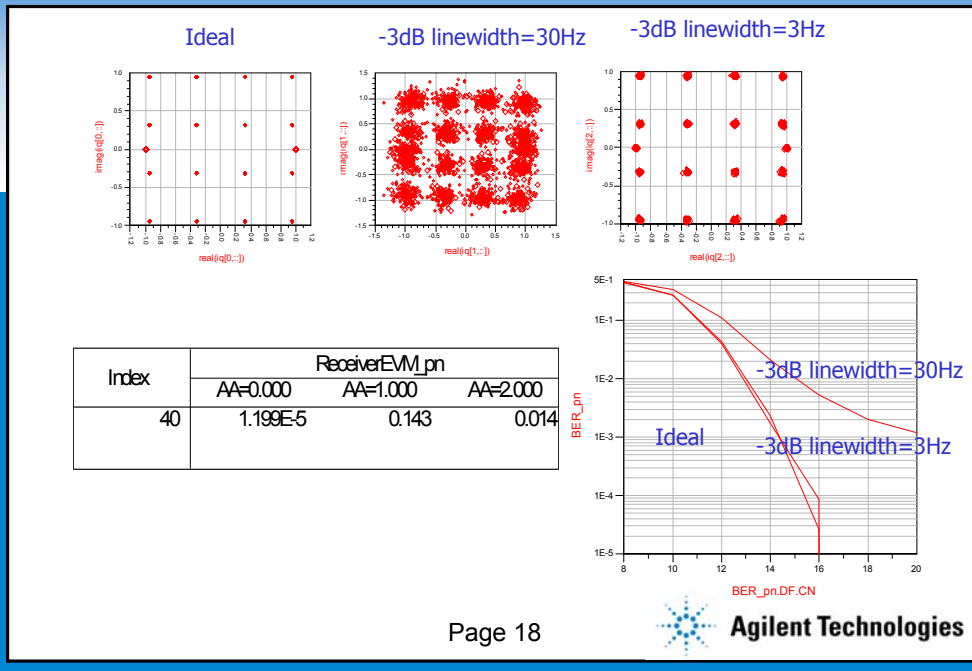
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This model for a local oscillator is a piece-wise construction of SSB phase noise. The noise will be created as a DSB spectrum within the analysis BW specified by the Tstep in the simulation. The spectrums shown are normalized to indicate the -3 dB bandwidth associated with integrating the phase noise power and comparing to the carrier power.

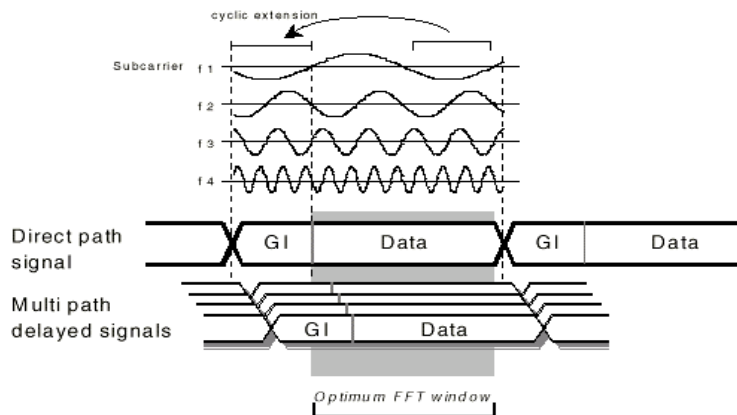
Effects of Oscillator Phase Noise



You can see that the ICI due to phase noise get worse as the phase noise spectrum BW (linewidth) becomes a larger percentage of the sub-carrier spacing.

Remember at lower phase noise SSB frequencies, the phase tracking capability of the OFDM receiver will correct the phase disturbance.

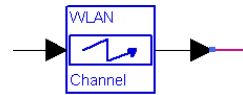
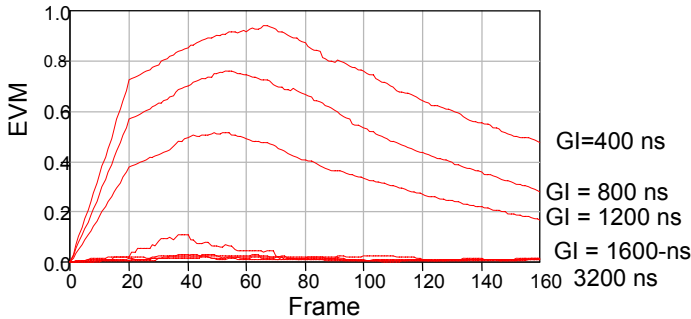
Guard Interval



- **Multipath delays up to the guard time - Inter-Symbol Interference**
- **Sub-carriers remain orthogonal for multipath delays up to guard time (no Inter-Carrier Interference)**

**Source: Basics and History of OFDM- Richard van Nee*

Guard Interval variation- Channel model



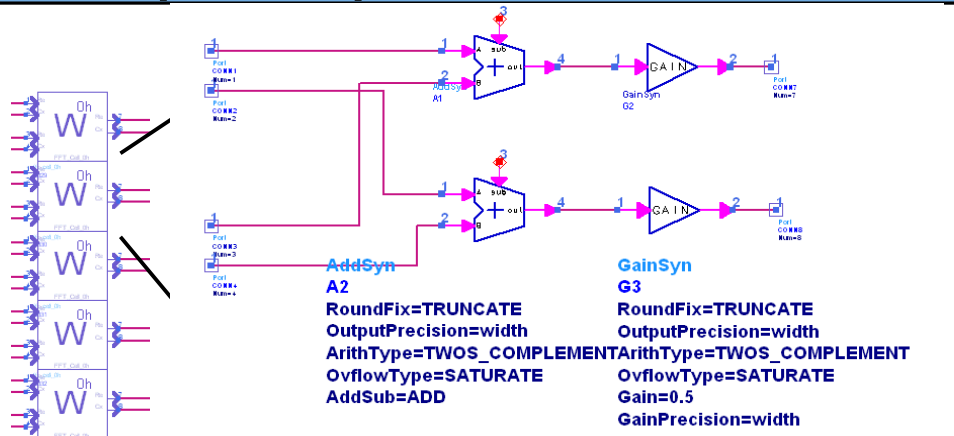
```
WLAN_ChannelModel
W64
ModelType=UserDefined
PathNumber=2
PowerArray="0.0 -5"
DelayArray="0.0 1000 "
FadingType=Rayleigh
RiceanFactor=10
Seed=1234567
N=10
Pathloss=No
Env=TypicalUrban
```

EVM vs. number of frames for variable Guard interval

it's for non-802.11a applications, since GI is fixed in standard. But if range extension is needed, GI increases, and those apps require flexible GI and simulation is important.

This is the test at 48 Mb/s

Fixed point implementation



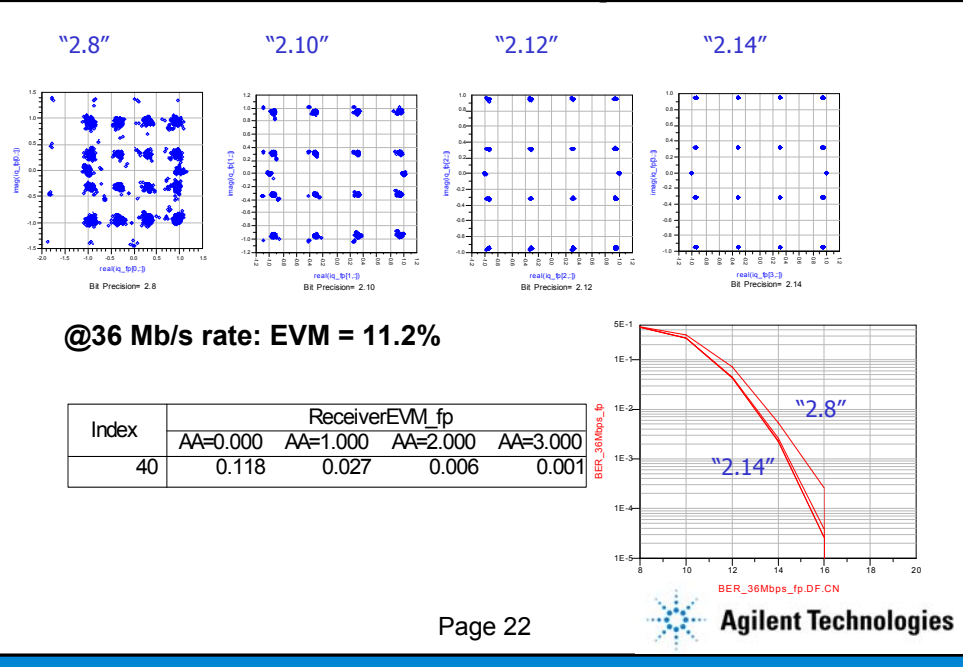
- 64-point IFFT/FFT in fixed-point arithmetic
- Decimation in Frequency, Radix-2 algorithm
- Bit precision of “2.8”, “2.10”, “2.12” and “2.14” simulated



This is where you get one step closer to HW. At the level of fixed point blocks.

This is where you can create HDL code as well.

Effects of Fixed Point Implementation



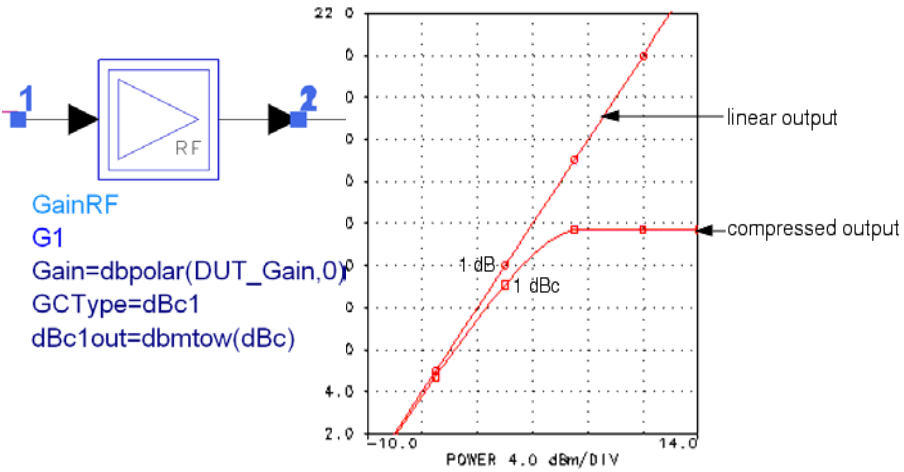
The simulation results show that as the wordlength of IFFT and FFT is reduced, the uncertainty associated with quantizing a QAM symbol will degrade the receiver performance. This is shown as both a degradation in EVM as well as a degradation in BER.

Reference:

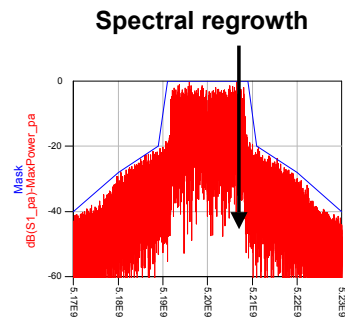
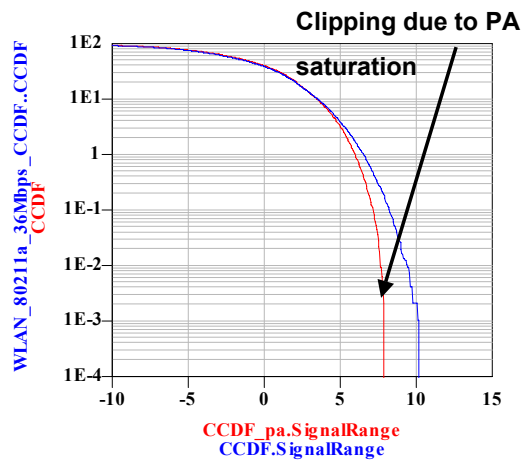
Impact of front end non-idealities on Bit Error Rate Performances of WLAN-OFDM transceivers- B. Come, R Ness et al

Power Amplifier- behavioral model

PA behavioral model used as a non-linear element



Effects Of Power Amplifier Non-linearity



GainRF
G1
Gain=dbpolar(DUT_Gain,0)
GCType=dBc1
dBc1out=dbmtow(dBc)

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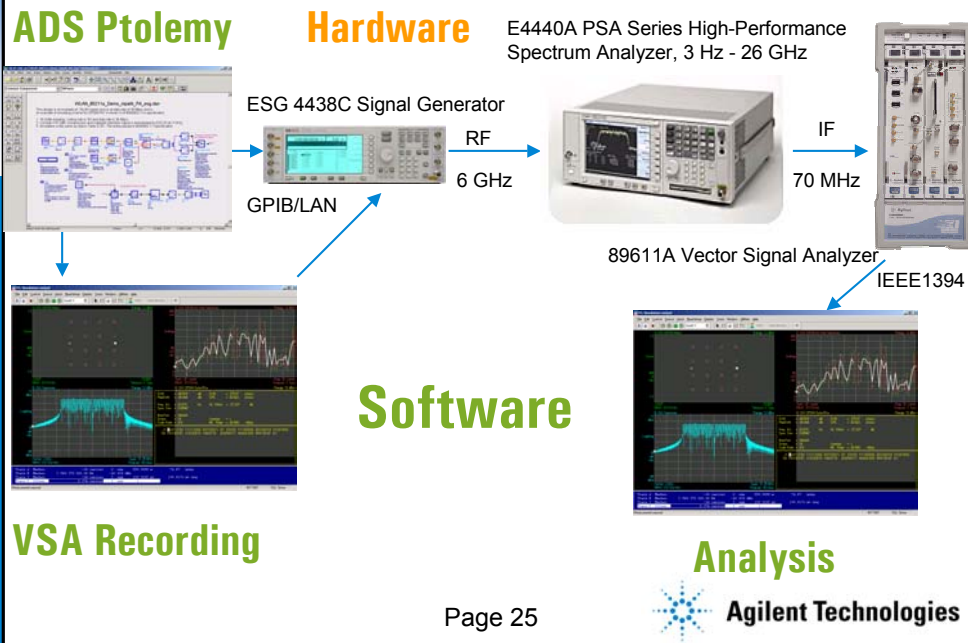
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We show that gain_RF behavioral model at the system level characterizes PA non-linearity by way of 1 dB compression point or level of back off.

-Before we treat the PA design and testing more rigorously

next we will revisit the instruments and the role they play early on in the design cycle for measurement and analysis of key parameters with in ADS environment

802.11a Design & Verification (6 GHz)



ADS 802.11a 16QAM modulation, 36 Mbps signal is simulated and analyzed with VSA software. Using ADS ESG-C links or the VSA hardware ESG-C links, download I and Q to the ESG dual-arbitrary waveform generator. The ESG hardware's 802.11a 6 GHz RF signal is analyzed by PSA/VSA. This allows ADS to emulate transmitter hardware. Radio impairments may include ISI, ICI, Phase Noise, PA nonlinearity, Multipath Delay Spread, or Power vs. Time.

ADS WLAN 802.11a - Nonlinear PA

The screenshot displays the ADS (Advanced Design System) interface for a WLAN 802.11a simulation. The main window shows a schematic diagram titled "WLAN_80211a_Demo_mpath_PA.dsn". The schematic includes various components such as signal sources, filters, amplifiers, and a nonlinear power amplifier (PA) block. A control panel titled "Agilent Ptolemy Control Panel" is overlaid on the right side of the schematic. This panel features a "Pause" button, a "Quit" button, a "Scale: 1.0" indicator, and a slider labeled "PA Backoff from 1 dBc" with a value of "0.0". Below the schematic, there is a list of simulation parameters and a status bar showing "Page 26" and the "Agilent Technologies" logo.

WLAN_80211a_Demo_mpath_PA.dsn

This design is an example of WLAN signal source at data rate of 38 Mbps and is an example of encoding a frame for OFDM PHY in Annex G of IEEE802.11a specific

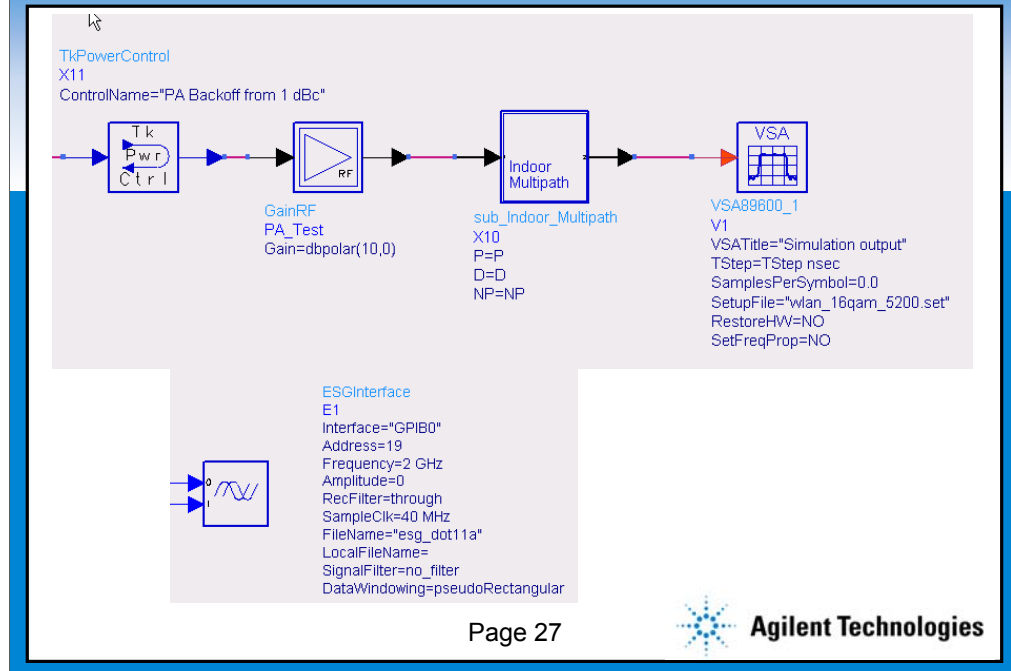
1. 16-QAM mapping, coding rate is 3/4 and data rate is 38 Mbps.
2. ADS includes complex PA compression, and multipath distortion. VSA equalizer removes multipath.
3. Simulation is the same as that in Table G.24 - The entire packet in IEEE802.11 Specification.

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ADS simulation includes complex PA compression (large-signal S21 amplitude and phase in compression) and multipath distortion. Note effect of linear multipath distortion on spectrum, which is removed by VSA equalizer.

An interactive slider controls PA back off from 1-dB compression point. Adjust PA drive level real-time to meet the required 802.11a EVM specifications. Nonlinear effects are not removed by equalizer.

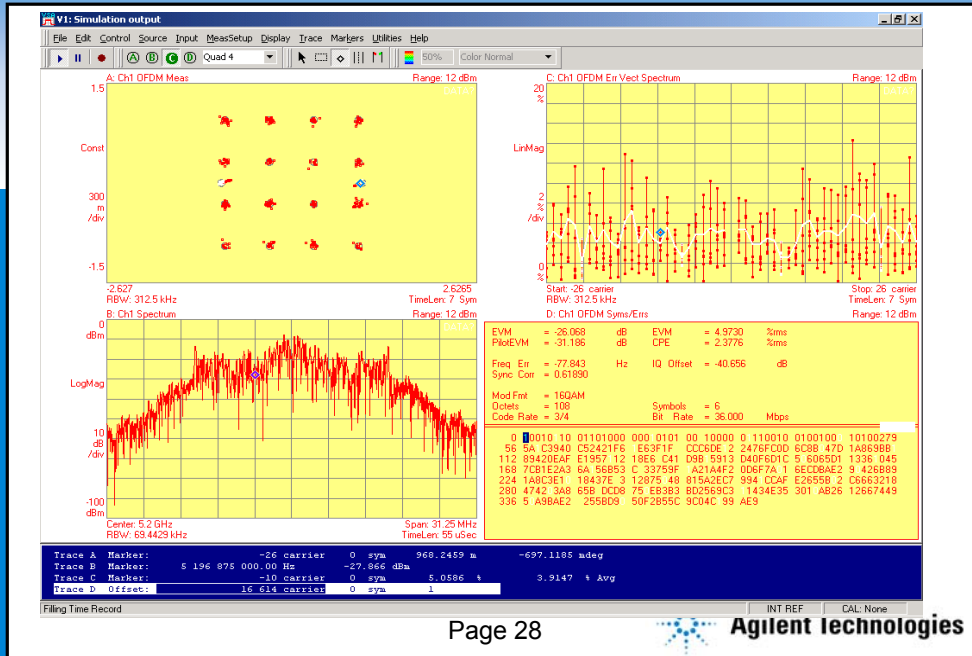
ADS WLAN 802.11a – VSA and ESG links



ADS simulation includes complex PA compression (large-signal S21 amplitude and phase in compression) and multipath distortion. Note effect of linear multipath distortion on spectrum, which is removed by VSA equalizer.

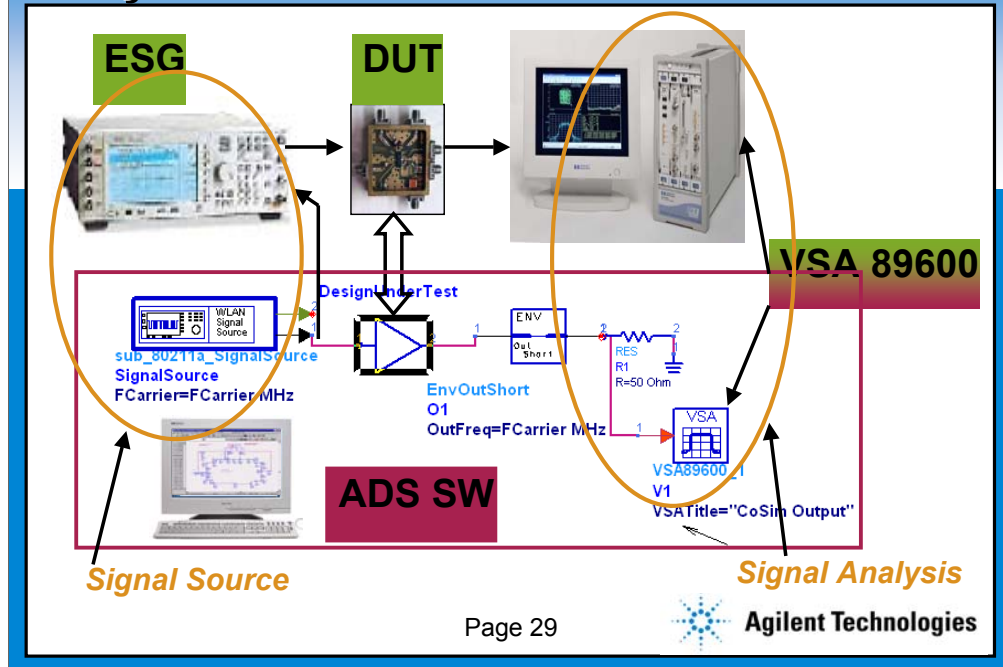
An interactive slider controls PA back off from 1-dB compression point. Adjust PA drive level real-time to meet the required 802.11a EVM specifications. Nonlinear effects are not removed by equalizer.

802.11a Signal with Multi-path and PA



ADS simulation with VSA link display for software only analysis. Note multi-path effects on spectrum, which are removed by VSA equalizer.

Early Verification Test Bench



Let's revisit ADS Design and Verification environment

Possibilities for this "Early Verification Test Bench"

include:

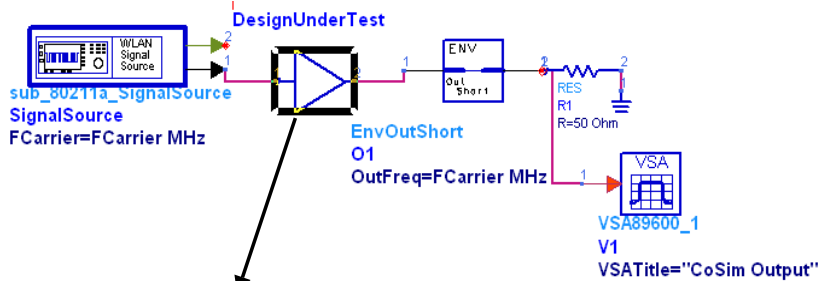
.Use simulation models or simulated circuit designs to fill-in for missing HW so verification testing can start earlier.

•Replace simulation models/circuits with hardware as fabrication progresses...verifying end-to-end performance of system at every stage

• Transition To & From design and test environment continuously to identify and fix issues early- where changes are easier/less costly to make

Power Amplifier Circuit Co-Simulation

Test Condition: Data rate =24 Mb/s and 54 Mb/s



@5.8 GHz
Nominal Gain= 11.4
P1dB = 21 dBm
Nominal Power = 17 dBm

Data Rate	*EVM, %
24	15.8
54	5.6

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here is an early sample of a Power Amp tuned at 5.8 GHz. From the Preliminary data - here are some of its characteristics:

Nominal Gain = 11.4

(1 dB compression point) = 21 dBm

Nominal power == 17 dBm

What we need to know is that given the circuit model how far can we drive the PA before the value of EVM(Error Vector Magnitude) breaks down- Two modes are tested:

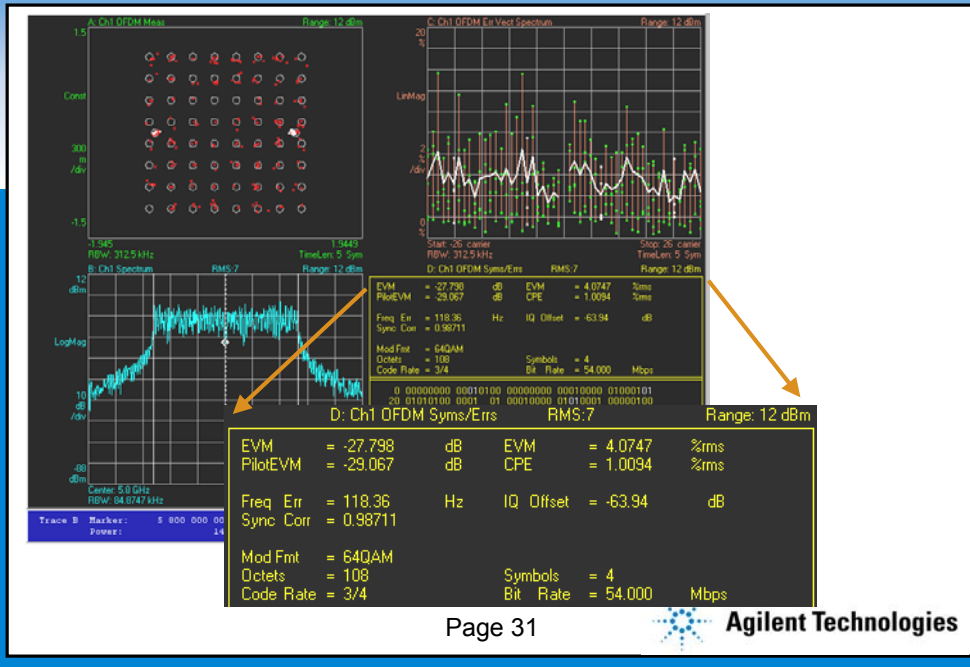
1- 24 Mb/s which needs to meet 15.8% EVM

2- 54 Mb/s needs to meet 5.6% EVM

So we need to sweep the input power and measure the corresponding EVM. Since the gain is 11.4 we elected not to exceed 6 dBm input power-

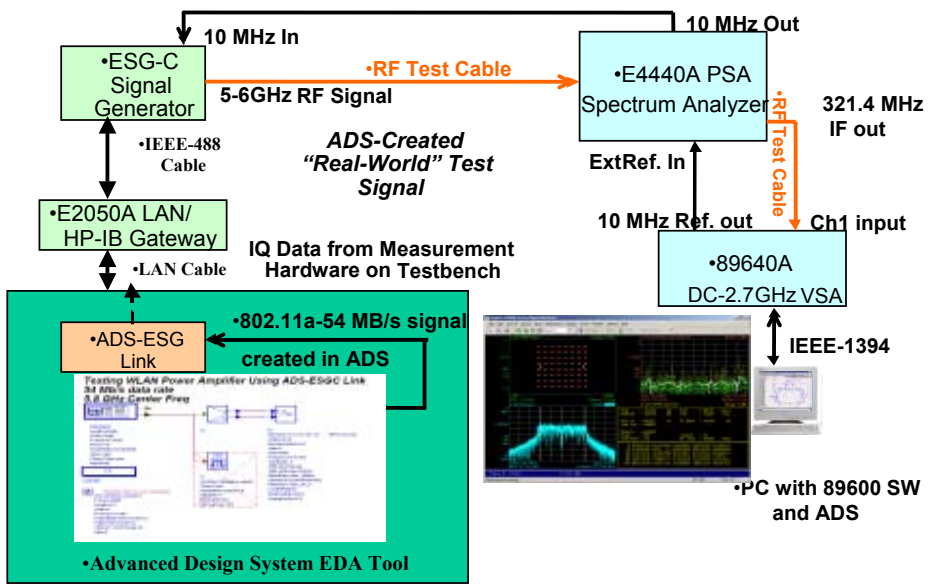
Notice that the PA circuit model is being simulated with Circuit Envelop and the signal source with Ptolemy data flow simulation and measurement is handled by VSA software simulation- simultaneously in ADS environment

Result of Co-simulation for 54 Mb/s



This shows 4.08% EVM

Connected Software and Hardware



Summary of results @ 24 Mbps, 5.8 GHz

Condition	EVM, dB	EVM, %	Comment
ADS/VSA, Pin = +5 dBm	-20.9	9.0	Pout=16.04 dBm
ADS/VSA, Pin = +6 dBm	-18.1	12.4	Pout=16.84 dBm
ADS/ESG-C/DUT/VSA #64, Pin = +5 dBm	-20	9.7	
ADS/ESG-C/DUT/VSA #64, Pin = +6 dBm	-18.2	12.6	

The specification EVM is 15.8 %.



Summary of results @54 Mb/s, 5.8 GHz

Condition	EVM, dB	EVM, %	Comment
ADS/VSA, Pin = +3 dBm	-27.8	4.08	Pout=14.41 dBm
ADS/VSA, Pin = +4 dBm	-24.5	5.9	Pout=15.14 dBm
ADS/ESG-C/DUT/VSA #64, Pin = +3 dBm	-25.1	4.8	
ADS/ESG-C/DUT/VSA #64, Pin = +4 dBm	-23.1	6.8	

The specification EVM is 5.6 %.

Summary

- System, RF, baseband and test engineers collaborate in a single environment: **ADS**
- ADS WLAN DVE provides:
 - **IEEE802.11a, Hiperlan2** compliant models
 - Configurable **Tx & Rx models** for all rates
 - Pre-configured **test benches**
 - **Design Guide** utility to browse impairment simulation setups
- Early verification with “**Connected Solution**”
- **PA** design was verified using HW prototype

> The ability to mix levels of abstraction, using detailed RF circuit and DSP designs, when available, and functional elements when detailed designs aren't available, allows the overall system performance to be evaluated at every stage in the design process to reduce risk.

> Performance measures dictated by 802.11a standard includes:

-EVM

-RF spectrum

-PER and BER

>Design Guide enable designer to check them against impairments and degradations caused by non-ideal circuits and components of real world.

>Use simulation models or simulated circuit designs to fill-in for missing HW so verification testing can start earlier. Replace simulation models/circuits with hardware as fabrication progresses...verifying end-to-end performance of system at every stage

Transition To & From design and test environment continuously to identify and fix issues early- where changes are easier/less costly to make

>We showed an early prototype of a PA tuned to 5.8 GHz for WLAN applications from Agilent semiconductor group.

Simulation results showed a very nice agreement with the HW.

EVM was the metric we closely measured. This is a measurement that a PA designer does not necessarily care to know when doing the circuit design. Yet a necessary one dictated by IEEE802.11a.

Furthermore, the “signal source” and “signal analysis” via VSA were shared between simulation and test bench.

PA designer at this stage can concentrate on modification of circuit design- As we observed in this case in order to meet the power requirements- next step could be to use a parallel configuration of two PA to increase power level at 54 Mb/s to 17 dBm

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